IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): SUZUKI et al.	Atty. Dkt.: 01-085-RCE
Serial No.: 09/675,209	Group Art Unit: 2814
Filed: September 29, 2000	Examiner: FARAHANI, Dana
Title: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	

Assistant Commissioner for Patents
Washington, D.C. 20231

Date: April 25, 2003

BRIEF ON APPEAL UNDER 37 C.F.R. § 1.192

Sir:

Appellants hereby submit their Brief on Appeal in triplicate under 37 C.F.R. § 1.192.

1. REAL PARTY IN INTEREST

The real party in interest is DENSO Corporation, the assignee by virtue of an assignment recorded September 29, 2000 at Reel/Frame 011187/0378.

2. RELATED APPEALS AND INTERFERENCES

There is no known related appeal or interference that will directly affect, that will be directly affected by, or that will have a bearing on the Board's decision on this appeal.

3. STATUS OF CLA

Claims 1-20 and 38-51 are pending in the present applic
attached Appendix. Claims 1-3, 5, 7-20 and 38-51 have been rejected
never been rejected but will be discussed in connection with claims 3 and 5, 6 have
11 was objected to in an Office Action issued January 30, 2003 for containing info. Claim
Applicants amended claim 11 to correct the informalities in an Amendment filed May 30,
However, the Examiner included the objection to claim 11 in the subsequent Final Rejection
issued July 26, 2002 and did not comment on Applicants' amendment to the claim. Applicants
therefore assume that the Examiner inadvertently again included the rejection and did not address
Applicants' earlier amendments to claim 11.

4. STATUS OF AMENDMENTS

All amendments submitted by Applicants have been entered.

5. SUMMARY OF THE INVENTION

The present invention is generally directed towards a semiconductor device, and more
specifically to an insulated gate bipolar transistor that is divided into cell blocks and that can
operate irrespective of defects in one or more of the cell blocks by rendering the defective cell
block(s) inoperative through gate pads, each of which corresponds to one of the cell blocks.
Once defective cell blocks are identified, only the gate electrodes of non-defective cell blocks are
connected to corresponding gate pads.

In general, there is a need to increase the capacity of electric current in integrated
insulated gate type bipolar transistor (IGBT) or DMOS chips. This can be done by increasing th

chip area. However, increasing the chip area increases waste and reduces yield when a defect occurs. The present invention therefore provides a way of salvaging chips that have defects.

According to the present invention and referring to FIGS. 1 and 2, a semiconductor device (shown as an n-channel type IGBT 1 in the figures for simplicity of explanation; however p-channel type IGBTs as well as other devices could be used) includes a semiconductor substrate 2 upon which a plurality of cell blocks 12 and a plurality of gate pads 16 are provided. As shown for example in FIG. 2, each cell block (see 12a-12e in FIG. 2) includes a plurality of transistor cells, and each of the transistor cells includes a gate electrode 8. The gate electrode 8 of each transistor cell is connected to other gate electrodes through a wiring layer 13 and is connected to a gate pad (see 16a-16e in FIG. 2) that is specific to the cell block. Therefore, for example, the gate electrodes 8 of the cell blocks 12a and 12b are electrically independent from each other.

Each cell block is independently tested for defects. For example, referring to FIG. 2, a withstand voltage between a gate electrode 8 and an emitter electrode 10 is measured by applying a voltage through each of the gate electrodes 8. A cell block is determined to be non-defective when the withstand voltage is equal to or greater than a predetermined voltage, and is determined to be defective when the withstand voltage is lower than the predetermined voltage (page 11, lines 1-18). The semiconductor substrate 2 is then marked to show which of the cell blocks 12a-12e are defective.

As shown in FIG. 3, the gate pads 16a, 16b, 16d and 16e of the non-defective cell blocks 12a, 12b, 12d and 12e are connected to the gate terminal 17 for the IGBT 1. The gate pad 16e of the defective cell block 12c is connected to a ground terminal 19 or to an emitter pad 15 of the IGBT 1 that is fixed at a ground potential (page 13, lines 25-27). When an external gate controlling signal is fed from the gate terminal 17 to the gate electrodes 8, only the elements in

the non-defective cell blocks 12a, 12b, 12d and 12e are operated, and the elements in the defective cell block 12c do not adversely affect the operation of the IGBT (page 14, lines 1-3).

Therefore, the present invention provides an IGBT 1 that can operate regardless of whether one or more of the cell blocks 12a-12e are defective.

6. ISSUES

The issues presented for review are:

(1) Whether claims 1-2 and 7 are anticipated by U.S. Patent No. 5,644,148 to Kinzer (Kinzer);

(2) Whether claims 40-42, 46 and 48-51 are anticipated by Kinzer and claims 43-45 and 47 are obvious over Kinzer;

(3) Whether claims 3-4 and 16-19 are obvious over Kinzer in view of U.S. Patent No. 6,329,692 to Smith and further in view of U.S. Patent No. 6,180,966 to Kohno et al. (Kohno);

(4) Whether claims 5 and 6 are obvious over Kinzer in view of U.S. Patent No. 6,160,305 to Sanchez;

(5) Whether claims 8-15 are obvious over Kinzer in view of U.S. Patent No. 4,631,569 to Calhoun;

(6) Whether claim 20 is obvious over Kinzer in view of Smith and Kohno and further in view of U.S. Patent No. 5,793,065 to Shinohe et al. (Shinohe);

(7) Whether claim 38 is obvious over Kinzer in view of Smith and further in view of U.S. Patent No. 6, 339,191 to Crane, Jr. (Crane); and

(8) Whether claim 39 is obvious over Kinzer in view of Smith and further in view of Crane.

7. GROUPING OF THE CLAIMS

Claims 1-2 and 7-15 stand or fall together.

Claims 3-4 and 16-19 stand or fall together.

Claims 5 and 6 stand or fall together.

Claim 20 stands alone.

Claim 38 stands alone.

Claim 39 stands alone.

Claims 40-51 stand or fall together.

8. ARGUMENTS WITH RESPECT TO ISSUES PRESENTED FOR REVIEW

A. PRIOR ART SUMMARY

The cited references will be summarized for the Board's convenience prior to arguments being presented.

(1) U.S. Patent No. 5,644,148 to Kinzer

Kinzer discloses a cellular IGBT device having an increased concentration region in the active region between closely spaced base regions. The increased concentration region permits an increase in the latch current of the device and a decrease in switching loss without significantly increasing the forward voltage drop and reducing breakdown voltage. The increased concentration region allows for an increase in the amount of lifetime killing radiation

applied to the device, which can lead to an increase in switching speed without increasing the forward voltage drop.

Specifically, Kinzer discloses an IGBT device as is known in the art, including a P^+ substrate 50 upon which N^+ and N^- layers 51, 52 are epitaxially formed. Deep N^+ drain enhancement diffusions 60-62 are implanted into the N^- layer 52 and implant regions become P^+ base regions 80-82. P^- shallow "shelves" 120-122 surround the P^+ base regions 80-82 and N^{++} source regions 130-132 diffuse within the P^+ base regions 80-82. A hexagonally shaped grid represented by gate oxide and polysilicon segments 110-112 and 113-115, respectively (col. 11, lines 45-51) is formed along the windows where the P^- "shelves" 120-122 meet and a continuous emitter electrode 160 is applied on top of the hexagonally shaped grid. Above this, an amorphous silicon layer 161 and a thin photopolyimide layer 162 are formed. The photopolyimide layer 162 is etched to expose an emitter pad and a gate pad (not shown).

Therefore, Kinzer discloses an IGBT including transistor cells for improving device performance. Kinzer does not, however, teach or suggest a plurality of gate electrodes formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks. In addition, Kinzer fails to teach or suggest equally dividing the transistor cells into a plurality of groups and a corresponding plurality of common gate electrodes having gate pads for the plurality of groups. Rather, Kinzer teaches a common gate electrode G, a common emitter electrode 160, and gate pads formed in the photopolyimide layer 162 that are not electrically independent (col. 6, lines 44-52 and col. 12, lines 53-63).

(2) U.S. Patent No. 6,329,692 to Smith

Smith discloses an integrated circuit and method for reducing parasitic bipolar effects during electrostatic discharges. As shown in FIG. 3, Smith discloses a resistor 26 that is coupled between the source of an N-channel transistor 24 and ground. A source injection current source 32 is used to direct some of the electrostatic discharge current through the resistor 26 to prevent forward biasing of the base-emitter junction of the transistor 24, which in turn causes snapback of the inherent parasitic bipolar device (col. 3, lines 45-53). More specifically, Smith discloses in FIG. 4 that a source injection bias circuit 33 includes a ground terminal V_{SS} that is connected to a gate of the transistor 42 and a gate terminal V_{DD} that is connected with a gate of the transistor 36. During normal operation, current leakage is minimized as the source injection bias circuit 33 places a source injector transistor 34 into a non-conductive state and other transistors are also substantially non-conductive. During a high voltage event, the source injection bias circuit 33 maintains the source injector transistor 34 in a conductive state to therefore act as a current source and to ultimately direct the high voltage current to V_{SS} and to V_{DD}.

However, Smith fails to teach or suggest a plurality of gate electrodes formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks. Also, Smith fails to teach a plurality of cell blocks that includes a first non-defective cell block and a second defective cell block, much less that a first gate pad connects the first non-defective cell block to the gate terminal and a second gate pad connects the second defective cell block to the ground terminal. Rather, the transistor 36 of Smith must be formed by a non-defective cell and should be appropriately operated as part of an electric circuit as shown in FIG. 4.

(3) U.S. Patent No. 6,180,966 to Kohno et al.

Kohno discloses a trench gate type semiconductor device including a main cell having trench gates (MAIN IGBT REGION of FIG. 1) wherein a main current flows and a current sensing cell having trench gates (SENSE IGBT REGION of FIG. 1) wherein a small detection current flows. The current in the main cell is determined based on the small sample current flowing through the current sensing cell according to the ratio of current flow in the current sensing cell and the main cell. The orientation of the crystal face at the surfaces of the side walls of the trench gates in the main cell is made equal or almost equal to that of the crystal face at the side walls in the trench gates in the current sensing cell (col. 4, lines 16-22). Therefore, Kohno discloses that the ratio of current flow in the current sensing cell to that in the main cell can be accurately set to a desired value and that current sensing accuracy is improved (col. 4, lines 46-58).

Although Kohno teaches an integrated circuit with a plurality of transistor cells, Kohno fails to teach or suggest a plurality of cell blocks provided on a semiconductor substrate, each cell block including a plurality of transistor cells. Also, Kohno fails to teach that the plurality of cell blocks includes a first non-defective cell block and a second defective cell block. Further, Kohno fails to teach or suggest that a first gate pad connects the first non-defective cell block to a gate terminal and a second gate pad connects the second defective cell block to a ground terminal.

(4) U.S. Patent No. 6,160,305 to Sanchez

Sanchez teaches a thermal sensing element 10 for an integrated circuit that incorporates a vertical PNP bipolar transistor 12 whose base current is amplified by the current amplification

factor BETA of the transistor 12. The current amplification factor BETA depends on the temperature of the transistor 12 and on the temperature of the integrated die that incorporates the transistor 12. The emitter of the transistor 12 is connected to the source and to the gate of transistor 16.

However, while the thermal sensing element in Sanchez prevents overheating of, and therefore damage to, a non-defective IC, it has nothing to do with enabling a device such as an IGBT to function properly even when the device includes a cell block that is defective due to manufacturing-related defects. Sanchez therefore fails to teach or suggest a plurality of cell blocks provided on a semiconductor substrate, each cell block including a plurality of transistor cells. Also, Sanchez fails to teach that the plurality of cell blocks includes a first non-defective cell block that is connected to the gate terminal and a second defective cell block that is connected to the emitter or source pad.

(5) U.S. Patent No. 4,631,569 to Calhoun

Calhoun discloses a method of reducing the number of masks utilized in fabricating complex multi-level integrated circuits. Specifically, Calhoun discloses an integrated circuit wafer 12 that is divided into a plurality of individual integrated circuit cells 14, each including a plurality of circuit elements and a plurality of signal connect members or pads 16. Calhoun discloses that the cells 14 are electrically tested and are labeled with numeric and letter symbols representative of particular defects (see col. 4, lines 25-47).

However, the cells 14 as defined by Calhoun are different from the cell blocks of the present invention. That is to say, the cell blocks of the present invention are used in combination to form a single semiconductor device. Calhoun, on the other hand, discloses that each cell 14

includes a plurality of circuit elements such as semi-conductor diodes, transistors, conductors, resistors, and capacitors (see col. 3, lines 36-39). Therefore, Calhoun fails to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks as defined by the present application and that the plurality of gate electrodes in each cell block are electrically independent from the gate electrodes of other cell blocks. In addition, Calhoun fails to teach or suggest a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, wherein each of the gate pads is connected to one of the gate electrodes of the corresponding cell block.

(6) U.S. Patent No. 5,793,065 to Shinohe et al.

Shinohe discloses an insulated-gate thyristor that has an insulated-gate transistor located at the carrier-releasing section and that can be turned off at high speed while maintaining good on-state characteristics. Shinohe also discloses that the use of elements having different threshold voltages reduces the adverse influence of threshold voltage difference among the elements.

However, Shinohe fails to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks and that the plurality of gate electrodes in each cell block are electrically independent from the gate electrodes of other cell blocks. Further, Shinohe fails to teach or suggest a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, each of the gate pads being connected to one of the gate electrodes of the corresponding cell block.

(7) U.S. Patent No. 6,339,191 to Crane, Jr. et al.

Crane discloses a semiconductor die carrier including a plurality of electrically insulative side walls 102b, a plurality of electrically conductive leads 103 extending from at least one of the side walls 102b, and a semiconductor die 101 connected with corresponding ones of the electrically conductive leads 103 (col. 4, lines 28-38). Crane also discloses transportation packaging for a substrate such as a carrier tray (col. 24, lines 43-55).

However, Crane does not teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks, or a plurality of gate pads on the substrate, each gate pad being connected to the plurality of gate electrodes of the corresponding cell block. In addition, Crane does not teach or suggest that the plurality of chips is sorted based on an arrangement position of a defective cell block, much less that the defective cell block has a corresponding gate pad that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential.

B. ARGUMENTS

(1) Whether claims 1-2 and 7 are anticipated by Kinzer.

Applicants submit that claims 1-2 and 7-15 are patentable as a separate group because the cited art fails to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks and that the plurality of gate electrodes in each cell block are electrically independent from the gate electrodes of other cell blocks.

Since claims 1-2 and 7-15 stand or fall together, independent claim 1 will be used as an exemplary claim in the following discussion.

Claim 1 recites, *inter alia*:

> a plurality of cell blocks provided on the semiconductor substrate, wherein each cell block includes a plurality of transistor cells;
>
> a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block are electrically independent of the plurality of gate electrodes of other cell blocks; and
>
> a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to one of the plurality of gate electrodes of the corresponding cell block.

The configuration as recited in claim 1 provides for blocks of transistor cells (cell blocks) on the semiconductor substrate. Each cell block includes a plurality of gate electrodes that are not connected to the gate electrodes of other cell blocks. The gate electrodes of each cell block are connected to a gate pad that corresponds to the particular cell block and that is provided on the semiconductor substrate.

In the Final Rejection dated July 26, 2002 (hereinafter "the Final Rejection"), the Examiner rejected claims 1, 2 and 7 (along with claims 40-42, 46, and 48-51 to be discussed later) under 35 U.S.C. §102(b) as being anticipated by Kinzer. Specifically, the Examiner stated that "[R]egarding claim 1, Kinzer discloses, figure 19, a semiconductor substrate 52; a plurality of cell blocks provided on the semiconductor substrate; a plurality of gate electrodes G electrically independent of one another and respectively provided in the plurality of cell blocks; and a plurality of gate pads (not shown) are provided on the semiconductor substrate and respectively connected with the plurality of gate electrodes (see column 12, lines 60-65)."

However, Applicants respectfully assert that Kinzer does not disclose a plurality of cell blocks comprised of transistor cells. Although Kinzer discloses an IGBT with a plurality of

identical cells (see col. 8, lines 60-65), it fails to disclose that these cells are grouped into cell blocks. Further, Kinzer fails to disclose a plurality of gate electrodes that are formed in each of the plurality of cell blocks and that are electrically independent from the pluralities of gate electrodes formed in other cell blocks. Rather, Kinzer discloses a common gate electrode connected to all gates. Specifically, even though not well shown in the two-dimensional depiction of the IGBT device in FIG. 19, the gate electrodes are interconnected as discussed in column 11, lines 45-51, which explains manufacturing processes of a semiconductor device illustrated in FIG. 15, and ultimately in FIG. 19 (see col. 8, lines 60-63):

> As shown in FIG. 15, this exposes the remaining ***polysilicon web*** and the surface of the silicon substrate 52 inside the windows 98, 99 and 100. Note that this photolithograph-etch step leaves in place oxide islands 83, 84 and 85, as well as the ***hexagonally shaped grid represented by gate oxide and polysilicon segments respectively 110, 111, 112 and 113, 114, 115***. [emphasis added]

This interconnection configuration is also described in column 6, lines 42-47 of Kinzer in connection with FIG. 2, which states as follows:

> The gate segments 31, 32 and 33 will be connected to an appropriate common gate pad (not shown). For purposes of illustration, ***a gate electrode "G" is shown connected to segment 3, it being understood that this gate electrode will be connected to all of the gate segments of the entire gate mesh***. [emphasis added]

Therefore, referring specifically to the language of claim 1, Kinzer fails to show a plurality of cell blocks provided on the semiconductor substrate, wherein each cell block includes a plurality of transistor cells, and a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block are electrically independent of the gate electrodes of other cell blocks.

Further, Applicants respectfully assert that Kinzer does not disclose a plurality of gate pads on the semiconductor substrate corresponding to a plurality of cell blocks and each being

connected to one of the gate electrodes of the corresponding cell block. As discussed above, Kinzer merely discloses a semiconductor device having a common gate electrode connected to all of the gates.

In his §102(b) rejection, the Examiner continued "[r]egarding claim 2, see figure 18." Applicants believe this was intended to indicate that FIG. 18 of Kinzer discloses the features recited in claim 2. However, as discussed above in connection with claim 1, Kinzer does not disclose a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, much less the particular arrangement of the gate pads that is recited in claim 2. Specifically, Applicants' claim 2 recites "the plurality of gate pads are arranged along a side of the semiconductor substrate." Applicants assert that FIG. 18 shows neither a plurality of cell blocks nor a plurality of gate pads. Rather, FIG. 18 discloses a substrate 52 including: P^+ regions 80, 81 and 82; N^{++} regions 130, 131 and 132; and deep N^+ regions 60, 61 and 62. FIG. 18 also discloses that gate oxide segments 110, 111 and 112, oxide segments 83, 84 and 85, and polysilicon segments 113, 114 and 115 are located on top of the substrate 52 and are covered by an interlayer silicon dioxide coating 140. The polysilicon segments 113, 114 and 115 ultimately become gate electrodes and would each therefore be located within a cell. However, Kinzer fails to disclose grouping the cells into cell blocks. In addition, there is no mention in Kinzer, specifically regarding FIG. 18, which teaches or suggests gate pads that correspond to each cell block.

In summary, Applicants respectfully submit that Kinzer does not show or suggest all elements of the claimed invention(s) and therefore does not anticipate claim 1 under 35 U.S.C. §102(b). Based on the comments above and in view of the evidence presented, Applicants respectfully submit that independent claim 1 and its dependent claims 2 and 7 are patentable

under 35 U.S.C. §102(b) over Kinzer. The Examiner's rejection of claims 1, 2 and 7 on these grounds is therefore improper and should be reversed.

(2) Whether claims 40-42, 46 and 48-51 are anticipated by Kinzer and claims 43-45 and 47 are obvious over Kinzer.

Applicants submit that claims 40-51 are patentable as a separate group because the cited art fails to teach or suggest a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups, a plurality of common gate electrodes for the plurality of groups, and a plurality of gate pads for the plurality of common gate electrodes.

Since claims 40-51 stand or fall together, independent claim 40 will be used as an exemplary claim in the following discussion.

Claim 40 recites, *inter alia*:

> ... a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups;
> a plurality of common gate electrodes for the plurality of groups, respectively; and
> a plurality of gate pads for the plurality of common gate electrodes, respectively.

The configuration as recited in claim 40 provides for a plurality of common gate electrodes and a plurality of gate pads for a plurality of equal groups of transistor cells on a semiconductor chip.

In addition to claims 1, 2 and 7 discussed above, the Examiner rejected claims 40-42, 46, and 48-51 under 35 U.S.C. §102(b) as being anticipated by Kinzer in the Final Rejection. Specifically, the Examiner stated that Kinzer discloses in FIG. 2 a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups, a plurality of

common gate electrodes for the plurality of groups, and a plurality of gate pads for the plurality of common gate electrodes.

Although Applicants agree that Kinzer does disclose transistor cells on a semiconductor chip, Applicants respectfully assert that, contrary to the Examiner's statement, Kinzer fails to disclose that the transistor cells are divided into groups of cells on a semiconductor chip, much less that the cells are equally divided into groups of cells. In addition, as discussed above in connection with claim 1, Kinzer fails to disclose a plurality of common gate electrodes for the plurality of groups, respectively, thus implying that each group has a separate common gate electrode. Rather, Kinzer discloses that the gate electrodes are all interconnected. Further, Applicants respectfully assert that Kinzer does not disclose a plurality of gate pads on the semiconductor substrate and respectively connected with the plurality of gate electrodes.

Further regarding claim 42, which depends from claim 40 and from which claims 46 and 48 depend, Kinzer fails to disclose an equipotential pad that has a source potential and that is adjacent to a plurality of gate pads or a possibly defective transistor cell. On page 3, lines 14-15 of the Final Rejection, the Examiner has alleged that in FIG. 2 there is a pad that is non-numbered and that is adjacent to the plurality of gate pads (not shown). Applicants respectfully assert that the object to which the Examiner refers is merely a connector to the emitter electrode 40 (see column 6, lines 48-52) and is not an equipotential pad. In addition, there is no indication in the Kinzer disclosure that the object in FIG. 2 is adjacent to a plurality of gate pads, especially since Kinzer does not disclose a plurality of gate pads.

In summary, Applicants respectfully submit that Kinzer does not show or suggest all elements of the claimed invention(s) and thus does not anticipate claim 40 under 35 U.S.C. §102(b). Based on the comments above and in view of the evidence presented, Applicants

respectfully submit that independent claim 40 and its dependent claims 41-42, 46 and 48-51 are patentable under 35 U.S.C. §102(b) over Kinzer. The Examiner's rejection of claims 40-42, 46 and 48-51 on these grounds is therefore improper and should be reversed.

In the Final Rejection, the Examiner also rejected claims 43-45 and 47 under 35 U.S.C. §103(a) as being unpatentable over Kinzer. Specifically, the Examiner stated that Kinzer discloses in FIG. 2 a gate terminal G, a source terminal connected to the upper left hand side of source electrode 40, and drain terminal connected to the bottom drain electrode 41. The Examiner stated that Kinzer discloses in FIG. 19 a gate terminal G that is connected to some of the gate pads.

Claims 43-45 and 47 depend from claim 40. As discussed above in connection with the 35 U.S.C. §102(b) rejection of claim 40, Kinzer fails to teach or suggest a plurality of equal groups of transistor cells on a semiconductor chip, a plurality of common gate electrodes for the plurality of groups and a plurality of gate pads for the plurality of common gate electrodes. Rather, as discussed above, Kinzer does not teach the grouping of transistor cells and teaches a single gate pad for a common emitter.

In view of the above arguments with respect to claim 40, from which claims 43-45 and 47 depend, Applicants respectfully request that the rejection under 35 U.S.C. §103(a) of claims 43-45 and 47 be withdrawn.

(3) Whether claims 3-4 and 16-19 are obvious over Kinzer in view of Smith and further in view of Kohno.

Applicants submit that dependent claims 3-4 and 16-19 are patentable as a separate group because the cited art fails to teach or suggest a gate terminal provided outside of the

semiconductor substrate, the gate terminal being electrically independent of the ground terminal, a plurality of cell blocks including a first non-defective cell block and a second non-defective cell block, and a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacent to the plurality of gate pads.

In the Final Rejection, the Examiner rejected claims 3 and 16-19 under 35 U.S.C. §103(a) as being obvious over Kinzer in view of Smith and further in view of Kohno. Specifically, the Examiner stated that Kinzer discloses the claimed invention except for a ground and a gate terminal to be connected to the semiconductor device. The Examiner indicated that Smith discloses transistors 42 and 36, the gates of which are connected to a ground terminal V_{SS} and a gate terminal V_{DD}, respectively. In addition, the Examiner indicated that Kohno discloses a plurality of cell blocks in FIG. 2 in which the over current can damage the cells.

Although not stated by the Examiner, Applicants will assume that claim 4 is also subject to this rejection since claim 4 depends from claim 3 and is not otherwise rejected.

Since claims 3-4 and 16-19 stand or fall together, dependent claim 3 will be used as an exemplary claim in the following discussion.

Claim 3 recites, *inter alia*:

> 3. The semiconductor device according to claim 1, further comprising:
> a ground terminal provided outside of the semiconductor substrate; and
> a gate terminal provided outside of the semiconductor substrate, the gate terminal being electrically independent of the ground terminal, wherein:
> the plurality of cell blocks includes a first non-defective cell block and a second defective cell block; and
> the plurality of gate pads includes a first gate pad that connects the first non-defective cell block to the gate terminal, and a second gate pad that connects the second defective cell block to the ground terminal.

The configuration as recited in claim 3 for a non-defective first cell block that is connected to a gate terminal and a defective second cell block that is connected with a

ground terminal. Therefore, a gate controlling signal is not fed to the gate electrode of the defective cell block so that elements in the defective cell block are not operated.

Applicants respectfully assert that, contrary to the Examiner's statement, Kinzer does not disclose the invention as claimed in independent claim 1, from which claims 3 and 16-19 depend. As discussed above, for example, Kinzer fails to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks. Also, Kinzer fails to disclose the specific features recited in dependent claim 3 such as, for example, a plurality of cell blocks that includes a first non-defective cell block and a second defective cell block and, as mentioned by the Examiner, a ground terminal and a gate terminal provided outside of the semiconductor substrate.

Smith discloses in FIG. 4 that a gate of the transistor 42 connects with a ground terminal V_{SS} via resistor 44, and a gate of the transistor 36 connects with a gate terminal V_{DD}. However, the transistor 42 connected to the ground terminal V_{DD} must be formed by a non-defective cell and should be appropriately operated as part of an electric circuit as shown in FIG. 4. Therefore, claim 3, which recites that "a second gate pad that connects the second defective cell block to the ground terminal" is not taught or suggested by Smith. In addition, Smith fails to overcome the deficiencies of Kinzer by failing to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks.

Kohno discloses in FIG. 2 a plurality of cell blocks in which the over current can damage the cells. However, a cell block of the present invention may become defective during the substrate formation process. Damage caused by over current flowing in the cells, as disclosed by

Kohno, represents a different type of damage as opposed to the damage that would result in the plurality of cell blocks in the present invention if gates of defective cell blocks were connected with gates of non-defective cell blocks. The circuit as disclosed by Kohno is a preventative measure to keep over current from damaging cells once the semiconductor device is being used. The configuration as recited in claim 3 is for disabling defective cell blocks without having to discard the entire chip when a defect is present.

Applicants respectfully assert that there is no motivation to combine the circuitry of Kohno to cure the deficiencies of Kinzer, as Kohno is directed to the prevention of over current damage to the IC, while the semiconductor device of the present invention is designed to overcome problems associated with existing manufacturing defects. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. (See In re Vaeck, 947 F.2d 488 (Fed. Cir. 1991), cited in MPEP 2142, Aug. 2001.)

In addition, the cell blocks as provided for in Kohno differ from those recited in independent claim 1, from which claim 3 depends. Specifically, the cell blocks provided on a semiconductor substrate of Kohno do not each include a plurality of transistor cells. Also, Kohno fails to teach that the plurality of cell blocks includes a first non-defective cell block and a second defective cell block, much less that a first gate pad connects the first non-defective cell clock to a gate terminal and a second gate pad connects the second defective cell block to a ground terminal.

Accordingly, Kinzer, Smith and Kohno fail to teach or suggest all features of the present invention as recited in claims 1 and 3 such as, for example, a plurality of cell blocks including a plurality of transistor cells wherein gate electrodes of one cell block are independent from the

gate electrodes of other cell blocks. Kinzer, Smith and Kohno also fail to teach or suggest a first gate pad that connects a first non-defective cell block to a gate terminal, and a second gate pad that connects a second defective cell block to a ground terminal as recited in dependent claim 3. Thus, even if Smith and Kohno were combined with Kinzer, the present invention as recited in the claims would still not be taught or suggested by the prior art combination.

In addition, Applicants respectfully assert that there is no motivation to combine the Kinzer, Smith and Kohno references as they are used for completely different purposes. The IGBT device disclosed by Kinzer is directed to reducing the switching loss without reducing breakdown voltage or increasing forward voltage drop. The circuit disclosed by Smith is directed to reducing parasitic bipolar effects during electrostatic discharges. The semiconductor device disclosed by Kohno is directed to the prevention of over current damage to an IC. Rather, it appears that the combination of Kinzer, Smith and Kohno presented by the Examiner is tantamount to a reconstruction of the claimed invention by picking references from diverse arts and using Appellant's invention as a blue print to make the combination.

Further regarding claim 16, claim 16 also depends from claim 1 and further recites a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacent to the plurality of gate pads. The Examiner stated on page 4 of the Final Rejection that Smith discloses an emitter potential 32 in FIG. 3 on the semiconductor substrate. However, Kinzer, Smith and Kohno fail to teach or suggest a plurality of pads having an emitter potential. Having a number of pads to correspond with the cell blocks allows the potentials of the different emitter electrodes (as recited in claim 1) to be separately accessible.

Claim 17 depends from claim 16 and further recites a gate terminal provided outside of the semiconductor substrate and that the plurality of cell blocks includes a first non-defective cell

block that is connected with the gate terminal and a second defective cell block that is connected with one of the plurality of pads having an emitter potential. As discussed above in connection with claims 1 and 3, Kinzer fails to disclose a first cell block that is non-defective and a second cell block that is defective. Kinzer therefore also fails to disclose that the first cell block is connected with the gate terminal and that the second cell block is connected with a pad having an emitter potential. Although, as noted by the Examiner, Smith does disclose a terminal 24 outside the substrate, this terminal is not connected to a defective cell, since, as discussed above in connection with claim 3, Smith fails to teach or suggest that any of the transistors are defective or include defective cells. This deficiency is not overcome by Kohno, which also fails to teach or suggest a connection between a second defective cell block and a pad having an emitter potential.

Claims 18 and 19 directly depend from, and therefore include the limitations of, dependent claim 17. Therefore, claims 18 and 19 indirectly depend from claim 16 and ultimately from claim 1. Each of claims 1, 16 and 17, recites features not taught or suggested by Kinzer, Smith and Kohno.

Therefore, Applicants respectfully submit that claims 3-4 and 16-19 are not obvious in view of Kinzer, Smith and Kohno, considered individually or in combination. Based on the comments above regarding independent claim 1, Applicants respectfully submit that claims 3-4 and 16-19 are not obvious under 35 U.S.C. §103(a) in view of the three-way combination of Kinzer, Smith and Kohno. The Examiner's rejection of claims 3-4 and 16-19 on these grounds is therefore improper and should be reversed.

(4) Whether claims 5 and 6 are obvious over Kinzer in view of Sanchez.

In the Final Rejection, the Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Sanchez. Specifically, the Examiner stated that Kinzer discloses the invention except for an emitter pad and a source pad with the connection the Applicants disclose. The Examiner indicated that Sanchez discloses that a gate terminal of transistor 20 and an emitter terminal 12 have an emitter potential, and that a source pad is connected to the emitter in FIG. 1.

Although not stated by the Examiner, Applicants will assume that claim 6 is also subject to this rejection since claim 6 depends from claim 5 and is not otherwise rejected.

Applicants respectfully assert that the above arguments in connection with claim 1 show that Kinzer does not disclose the invention as disclosed in claim 1, from which claim 5 depends. Kinzer fails to disclose, for example, a plurality of cell blocks including a plurality of transistor cells and wherein gate electrodes of one cell block are independent from those of other cell blocks as recited in independent claim 1.

However, assuming *arguendo* that Kinzer discloses the invention except for an emitter pad and a source pad with the connection recited in claim 5 as alleged by the Examiner, the combination of Kinzer and Sanchez still does not render Applicants' invention obvious, as Sanchez fails to overcome the shortcomings of Kinzer. Specifically, Sanchez discloses in FIG. 1 that a gate of a transistor 20 connects with an output terminal, and a gate of the transistor 16 connects with an emitter terminal of the transistor 12, to create an emitter potential. However, the transistor 16 must be formed by a non-defective cell and should be appropriately operated as part of an electric circuit shown in FIG. 4. This is contrary to Applicants' claim 5, which recites that a second gate pad connects a defective cell block to the emitter or source pad.

Thus, even if Sanchez was combined with Kinzer, the present invention as recited in claim 5 would not be taught or suggested by the prior art combination for the same reasons discussed above in connection with claim 1. Applicants respectfully submit that claim 5 is patentable under 35 U.S.C. §103(a) over Kinzer and Sanchez. The Examiner's rejection of claim 5 and its dependent claim 6 on these grounds is therefore improper and should be reversed.

(5) Whether claims 8-15 are obvious over Kinzer in view of Calhoun.

In the Final Rejection, the Examiner rejected claims 8-15 under 35 U.S.C. §103(a) as being obvious over Kinzer in view of Calhoun. Specifically, the Examiner stated that Kinzer discloses the claimed invention except for a plurality of marks provided at a plurality of regions of the semiconductor substrate for determining the defectiveness of the particular cells. The Examiner has indicated that Calhoun discloses a plurality of circuit cells in which the defective cells are marked to be distinguished from the working cells.

However, as discussed above, Kinzer does not disclose the invention as claimed in independent claim 1, from which claims 8-15 depend. For example, Kinzer fails to teach or suggest a plurality of gate electrodes that are formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks. Also, Kinzer does not disclose a plurality of gate pads on the semiconductor substrate and respectively connected with the plurality of gate electrodes.

Calhoun discloses a plurality of circuit cells in which the defective cells are marked to be distinguished from the working cells. However, Calhoun fails to disclose a plurality of gate electrodes that are formed in each of a plurality of cell blocks, the plurality of gate electrodes in each cell block being electrically independent from the gate electrodes of other cell blocks. In

addition, the cells as disclosed in Calhoun differ from the cell blocks as recited in independent claim 1. That is to say, the cell blocks of the present invention are used in combination to form a single semiconductor device. Calhoun, on the other hand, discloses that each cell includes a plurality of circuit elements such as semi-conductor diodes, transistors, conductors, resistors, and capacitors (see col. 3, lines 36-39). In other words, a cell block of the claimed invention could be a component of one of the transistors that is a component of a cell block as disclosed by Calhoun. Therefore, the marks for discriminating whether a corresponding cell block is defective as recited in claim 8 are used for a different purpose than the marks of Calhoun since the purpose of the corresponding cell blocks differs.

Therefore, Applicants respectfully submit that claims 8-15 are not obvious in view of Kinzer and Calhoun, considered individually or in combination. Based on the comments above regarding independent claim 1, from which claims 8-15 depend, Applicants respectfully submit that claims 8-15 are patentable under 35 U.S.C. §103(a) over Kinzer in view of Calhoun. The Examiner's rejection of claims 8-15 on these grounds is therefore improper and should be reversed.

(6) Whether claim 20 is obvious over Kinzer in view of Smith and Kohno and further in view of Shinohe.

Claim 20 recites that the plurality of cell blocks includes a first group of cell blocks, which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks, which have different threshold voltages from one another and are connected with one of the plurality of pads. That is, the first group of non-defective cell blocks is connected with the gate terminal, while the second group of defective cell blocks is connected

with the pads with an emitter potential. Therefore, elements in the non-defective cell block are operated and elements in the defective cell block are not operated.

In the Final Rejection, the Examiner rejected claim 20 under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Smith and Kohno and further in view of Shinohe. Specifically, the Examiner stated that the combination of Kinzer, Smith and Kohno discloses the claimed invention except for the different threshold voltages of adjacent group of cells. The Examiner indicated that Shinohe discloses the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage difference among the elements.

However, in his conclusion that Kinzer, Smith and Kohno disclose the invention except for the different threshold voltages, the Examiner has relied on a number of previous arguments that Applicants believe to be moot in light of the above discussions. For example, the Examiner stated that Kinzer, Smith and Kohno disclose the invention as recited in claim 16. However, as discussed above in connection with claim 16, the combination of Kinzer, Smith and Kohno fails to teach or suggest all features of claim 16, from which claim 20 depends. For example, Kinzer, Smith and Kohno fail to teach or suggest a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacent to the plurality of gate pads. Having a number of pads to correspond with the cell blocks allows the potentials of the different emitter electrodes (as recited in claim 1) to be separately accessible.

In addition, Shinohe discloses that the use of adjacent elements having different threshold voltages reduces the adverse influence of threshold voltage differences among the elements. However, in such a configuration, the different threshold voltages are intentionally formed to reduce the adverse influence of the threshold voltage differences. This feature is different from

that recited in claim 20. Specifically, the present invention separates based on voltages to isolate good blocks from defective blocks rather than to average out voltage differences. Further, Shinohe fails to disclose a plurality of cell blocks including a plurality of transistor cells and wherein gate electrodes of one cell block are independent from those of other cell blocks as recited in independent claim 1. Therefore, Shinohe fails to cure the shortcomings of Kinzer, Smith and Kohno. Thus, even if these references were combined, the terms of the claims would not be satisfied by the resulting configuration.

Therefore, Applicants respectfully submit that claim 20 is not obvious in view of Kinzer, Smith, Kohno and Shinohe, considered individually or in combination. Based on the comments above regarding independent claim 1 and dependent claim 16, Applicants respectfully submit that claim 20 is patentable under 35 U.S.C. §103(a) over Kinzer, Smith, Kohno and Shinohe. The Examiner's rejection of claim 20 on these grounds is therefore improper and should be reversed.

(7) Whether claim 38 is obvious over Kinzer in view of Smith and further in view of Crane.

Applicants submit that claim 38 is patentable standing alone because the cited art fails to teach or suggest an apparatus for manufacturing an insulated gate type power IC including a chip transfer machine with a plurality of trays for selectively holding a plurality of chips, each chip including a semiconductor substrate upon which plurality of cell blocks are formed, each cell block including a plurality of gate electrodes that are electrically independent from those of others of the plurality of cell blocks.

Claim 38 recites *inter alia* blocks of transistor cells (cell blocks) on a semiconductor substrate. Each cell block includes a plurality of gate electrodes that are not connected to the gate electrodes of other cell blocks. The gate electrodes of each cell block are connected to one of a plurality of gate pads provided on the semiconductor substrate. Claim 38 also recites a chip transfer machine for selectively holding a plurality of chips and that the plurality of chips is sorted based on an arrangement position of a defective cell block of each chip in one of the plurality of trays. Claim 38 further recites that the defective block has a corresponding gate pad that is connected with one of a ground terminal and an emitter pad and that a non-defective cell block has a corresponding gate pad that is connected with a gate terminal provided outside the semiconductor substrate.

In the Final Rejection, the Examiner rejected claim 38 (and claim 39, to be discussed later) under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Smith and further in view of Crane. Specifically, the Examiner stated that Kinzer discloses a plurality of chips, each having a semiconductor substrate 20, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes G electrically independent of each other, and gate pads, connected with the gate electrodes. The Examiner indicated that Smith discloses in FIG. 4 a gate of transistor 42 connected to the ground, and gate of transistor 36 connected to a voltage potential. The Examiner also indicated that Crane discloses trays to carry dies. The Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate connections to the ground and a voltage in order to disable and enable the cells, respectively, and further to use trays in order to carry the chips.

However, contrary to the Examiner's statement, Kinzer does not teach or suggest a plurality of cell blocks on a substrate wherein each cell block includes a plurality of transistor

cells, a plurality of gate electrodes formed in each of the plurality of cell blocks wherein the gate electrodes of each cell block are electrically independent of the gate electrodes of other cell blocks, and a plurality of gate pads corresponding to the cell blocks.

As discussed above in connection with claim 1, Kinzer discloses a common gate electrode connected to all gates. Specifically, even though not well shown in the IGBT in FIG. 19 since FIG. 19 is a two-dimensional depiction, the gate electrodes are interconnected. Further, Applicants respectfully assert that Kinzer does not disclose a plurality of gate pads on the semiconductor substrate and respectively connected with the plurality of gate electrodes. As discussed above, Kinzer discloses a semiconductor device having a common gate electrode connected to all of the gates. However, Kinzer fails to disclose a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to one of the plurality of gate electrodes of the corresponding cell block.

Therefore, because Smith and Crane fail to overcome the deficiencies of Kinzer, such as, for example, a plurality of gate pads connected to a plurality of gate electrodes, the combination of Kinzer, Smith and Crane does not teach or suggest all features of the present invention. Further, although Crane teaches trays to carry dies the combination of Kinzer, Smith and Crane fails to teach or suggest a chip transfer machine including a plurality of trays for selectively holding a plurality of chips, the plurality of chips being sorted based on a position of a defective cell block, the defective cell block having a corresponding gate pad that is connected to either a ground terminal or an emitter pad, and a non-defective cell block of each of the plurality of chips having a corresponding gate pad that is connected with a gate terminal.

Thus, even if Crane was combined with Kinzer and Smith, the present invention as recited in claim 38 would not be taught or suggested by the prior art combination. Applicants respectfully submit that claim 38 is patentable under 35 U.S.C. §103(a) over Kinzer, Smith and Crane. The Examiner's rejection of claim 38 on these grounds is therefore improper and should be reversed.

(8) Whether claim 39 is obvious over Kinzer in view of Smith and further in view of Crane.

Applicants submit that claim 39 is patentable standing alone because the cited art fails to teach or suggest an insulated gate type power IC module that includes a plurality of insulated gate type ICs each including a semiconductor substrate upon which plurality of cell blocks are formed, each cell block including a plurality of gate electrodes that are electrically independent from the gate electrodes of other cell blocks. In addition, claim 39 recites that each of the insulated gate type ICs includes a defective cell block at an identical position and a non-defective cell block, the defective cell block having a corresponding gate electrode that is connected with a ground terminal or an emitter pad and the non-defective cell block having a corresponding gate electrode that is connected with a gate terminal.

In the Final Rejection, the Examiner rejected claim 39 under 35 U.S.C. §103(a) as being unpatentable over Kinzer in view of Smith and further in view of Crane. Specifically, the Examiner stated that Kinzer discloses a plurality of chips, each having a semiconductor substrate 20, a plurality of cell blocks provided on the semiconductor substrate, a plurality of gate electrodes G electrically independent of each other, and gate pads connected with the gate electrodes. The Examiner indicated that FIG. 4 of Smith discloses a gate of transistor 42

connected to the ground, and a gate of transistor 36 connected to a voltage potential. The Examiner also indicated that Crane discloses trays to carry dies. The Examiner alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to make the gate connections to the ground and a voltage in order to disable and enable the cells, respectively.

As discussed above in connection with claims 1 and 38, Kinzer fails to disclose certain of the patentable features of the present invention such as, for example, a plurality of electrically independent gate electrodes corresponding to a plurality of cell blocks and a plurality of gate pads on the semiconductor substrate and respectively connected with the plurality of gate electrodes. Smith and Crane do not overcome the deficiencies of Kinzer by teaching or suggesting a plurality of gate pads, nor do they teach or suggest an insulated gate type power IC module including a plurality of insulated gate type ICs, each including a defective cell block at an identical position.

Thus, even if Crane was combined with Kinzer and Smith, the present invention as recited in claim 39 would not be taught or suggested by the prior art combination. Applicants respectfully submit that claim 39 is patentable under 35 U.S.C. §103(a) over Kinzer, Smith and Crane. The Examiner's rejection of claim 39 on these grounds is therefore improper and should be reversed.

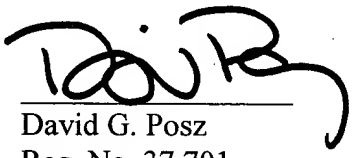
9. CONCLUSION

For the above reasons, claims 1-2, 7, 40-42, 46 and 48-51 are not anticipated by Kinzer, claims 43-45 and 47 are not obvious over Kinzer, claims 3-4 and 16-19 are not obvious over Kinzer in view of Smith and further in view Kohno, claims 5 and 6 are not obvious over Kinzer

in view of Sanchez, and claims 8-15 are not obvious over Kinzer in view of Calhoun. In addition, claim 20 is not obvious over Kinzer in view of Smith and Kohno and further in view of Shinohe and claims 38 and 39 are not obvious over Kinzer in view of Smith and further in view of Crane.

Therefore, Applicants respectfully submit that the Examiner's rejections of claims 1-20, 38-39 and 40-51 are improper and respectfully requests that the Examiner's rejections of the claims be REVERSED.

Respectfully submitted,



David G. Posz
Reg. No. 37,701

Posz & Bethards, PLC
11250 Roger Bacon Drive, Suite 10
Reston, VA 20190
(703) 707-9110
Customer Number: 23400

10. APPENDIX OF CLAIMS AS PENDING

The text of the claims on appeal is:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a plurality of cell blocks provided on the semiconductor substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block are electrically independent of the plurality of gate electrodes of other cell blocks; and

a plurality of gate pads provided on the semiconductor substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to one of the plurality of gate electrodes of the corresponding cell block.

2. (Amended) The semiconductor device according to claim 1, wherein:

the semiconductor substrate has a rectangular shape; and

the plurality of gate pads are arranged along a side of the semiconductor substrate.

3. (Amended) The semiconductor device according to claim 1, further comprising:

a ground terminal provided outside of the semiconductor substrate; and

a gate terminal provided outside of the semiconductor substrate, the gate terminal being electrically independent of the ground terminal, wherein:

the plurality of cell blocks includes a first non-defective cell block and a second defective cell block; and

the plurality of gate pads includes a first gate pad that connects the first non-defective cell block to the gate terminal, and a second gate pad that connects the second defective cell block to the ground terminal.

4. (Amended) The semiconductor device according to claim 3, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the ground terminal by one of wire-bonding, soldering, and pressure-welding.

5. (Amended) The semiconductor device according to claim 1, further comprising:

a gate terminal provided outside of the semiconductor substrate;

a source or emitter pad provided on the semiconductor substrate, wherein the source or emitter pad has a source potential or an emitter potential, wherein:

the plurality of cell blocks includes a first non-defective cell block and a second defective cell block; and

the plurality of gate pads includes a first gate pad that connects the first non-defective cell block to the gate terminal, and a second gate pad that connects the second defective cell block to the emitter or source pad.

6. (Amended) The semiconductor device according to claim 5, wherein:

the first gate pad is bonded to the gate terminal by one of wire-bonding, soldering, and pressure-welding; and

the second gate pad is bonded to the source or emitter pad by one of wire-bonding, soldering, and pressure-welding.

7. The semiconductor device according to claim 1, wherein the semiconductor substrate is an insulated gate type bipolar transistor chip.

8. (Amended) The semiconductor device according to claim 1, further comprising a plurality of marks provided at a plurality of regions of the semiconductor substrate, wherein the plurality of marks respectively corresponds to the plurality of cell blocks, each of the plurality of marks being for discriminating whether a corresponding cell block is defective.

9. (Amended) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by at least one of location, color, size, and shape of a corresponding one of the plurality of marks.

10. (Amended) The semiconductor device according to claim 8, wherein discrimination of whether each of the plurality of cell blocks is defective is determined by a number of the plurality of marks corresponding to each of the plurality of cell blocks.

11. (Amended) The semiconductor device according to claim 8, wherein:

the plurality of cell blocks includes a first cell block;

the plurality of gate pads includes a first gate pad connected with the first cell block; and

the plurality of marks includes a first mark for discriminating whether the first cell block is defective, the first mark being provided on a line passing through the first gate pad.

12. The semiconductor device according to claim 11, wherein the first mark is provided at a side of the first gate pad opposite to the first cell block.

13. (Amended) The semiconductor device according to claim 11, wherein:

the plurality of cell blocks includes a second cell block;

the plurality of gate pads includes a second gate pad connected with the second cell block;

the plurality of marks includes a second mark for discriminating whether the second cell block is defective, the second mark being located apart from a line passing through a center of the second gate pad.

14. (Amended) The semiconductor device according to claim 8, wherein each of the plurality of marks is located in a vicinity of a corresponding gate pad or on a surface of the corresponding gate pad.

15. The semiconductor device according to claim 8, wherein the plurality of marks can be recognized by an image recognition device of a wire-bonding apparatus.

16. (Amended) The semiconductor device according to claim 1, further comprising a plurality of pads having an emitter potential and provided on the semiconductor substrate adjacent to the plurality of gate pads.

17. (Amended) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor substrate, wherein:

the plurality of cell blocks includes a first cell block and a second cell block, the first cell block being non-defective and connected with the gate terminal and the second cell block being defective and connected with one of the plurality of pads having an emitter potential.

18. (Amended) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes;

a collector electrode provided on a back surface of the semiconductor substrate;

an emitter terminal bonded to the main surface of the semiconductor substrate and electrically connected with the plurality of emitter pads;

a collector terminal bonded to the back surface of the semiconductor substrate and electrically connected with the collector electrode; and

a resin member encapsulating the gate terminal, the emitter terminal, and the collector terminal together.

19. (Amended) The semiconductor device according to claim 17, further comprising:

a plurality of emitter electrodes respectively provided in the plurality of cell blocks;

a plurality of emitter pads provided on a main surface of the semiconductor substrate and respectively connected with the plurality of emitter electrodes; and

an emitter terminal provided outside of the semiconductor substrate and electrically connected with the emitter pads, wherein:

the first cell block is connected to the gate pad through a first bonding wire; and

the second cell block is connected to the one of the plurality of pads through a second bonding wire.

20. (Amended) The semiconductor device according to claim 16, further comprising a gate terminal provided outside of the semiconductor device, wherein:

the plurality of cell blocks includes a first group of cell blocks, which have an equal threshold voltage and are connected with the gate terminal, and a second group of cell blocks, which have different threshold voltages from one another and are connected with one of the plurality of pads.

38. (Amended) An apparatus for manufacturing an insulated gate type power IC, comprising:

a chip transfer machine including a plurality of trays for selectively holding a plurality of chips, wherein each chip includes:

a semiconductor substrate;

a plurality of cell blocks on the substrate, wherein each cell block includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the plurality of cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate and respectively corresponding to the plurality of cell blocks, wherein each gate pad is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

the plurality of chips is sorted based on an arrangement position of a defective cell block of each chip in one of the plurality of trays;

the defective cell block has a corresponding gate pad that is connected with one of a ground terminal having a ground potential and an emitter pad having an emitter potential; and

a non-defective cell block of each of the plurality of chips has a corresponding gate pad that is connected with a gate terminal provided outside of the semiconductor substrate.

39. (Amended) An insulated gate type power IC module that includes a plurality of insulated gate type ICs, each of the insulated gate type ICs comprising:

a semiconductor substrate;

a plurality of cell blocks located on the substrate each of which includes a plurality of transistor cells;

a plurality of gate electrodes formed in each of the cell blocks, wherein the plurality of gate electrodes of one cell block is electrically independent of the plurality of gate electrodes of others of the plurality of cell blocks; and

a plurality of gate pads on the substrate corresponding to the plurality of cell blocks, wherein each of the plurality of gate pads is connected to the plurality of gate electrodes of a corresponding cell block; wherein:

each of the insulated gate type ICs includes a defective cell block at an identical position and a non-defective cell block, the defective cell block having a corresponding gate electrode that is connected with one of a ground terminal provided outside of the semiconductor substrate and an emitter pad provided on the semiconductor substrate, the non-defective cell block having a corresponding gate electrode that is connected with a gate terminal provided outside of the semiconductor substrate; and

the insulated gate type power IC module is composed exclusively of the plurality of insulated gate type ICs.

40. A semiconductor device comprising:

a plurality of transistor cells arranged in a semiconductor chip and divided equally into a plurality of groups;

a plurality of common gate electrodes for the plurality of groups, respectively; and

a plurality of gate pads for the plurality of common gate electrodes, respectively.

41. The semiconductor device of claim 40, wherein each of the plurality of transistor cells comprises a source electrode on a surface side of the semiconductor chip and a drain electrode on a back side of the semiconductor chip, wherein each of the plurality of gate pads is located on the surface side of the semiconductor chip.

42. The semiconductor device according to claim 41, further comprising an equipotential pad adjacent to the plurality of gate pads, wherein a source potential is applied to the equipotential pad.

43. The semiconductor device according to claim 41, further comprising:

a gate terminal bonded to certain of the plurality of gate pads with wires;

a source terminal commonly soldered to the source electrode; and

a drain terminal commonly soldered to the drain electrode.

44. The semiconductor device according to claim 43, further comprising a coating of resin encapsulating the semiconductor chip, the wires, part of the gate terminal, and part of the drain terminal.

45. The semiconductor device according to claim 42, further comprising:

a gate terminal bonded to certain of the plurality of gate pads with wires;

a source terminal commonly soldered to the source electrode; and

a drain terminal commonly soldered to the drain electrode.

46. The semiconductor device according to claim 45, wherein the equipotential pad is provided for a gate pad corresponding to one of the plurality of groups including a possibly defective transistor cell to be bonded with a wire.

47. The semiconductor device according to claim 46, further comprising a coating of resin encapsulating the semiconductor chip, the wires, part of the gate terminal, and part of the drain terminal.

48. The semiconductor device according to claim 42, wherein the equipotential pad is provided for one of the plurality of gate pads corresponding to one of the plurality of groups including a possibly defective transistor cell to be bonded with a wire.

49. The semiconductor device according to claim 40, further comprising means for preventing one of the plurality of groups that includes a possibly defective transistor cell from operating.

50. The semiconductor device according to claim 49, wherein the preventing means includes means for applying a ground potential or a source potential to a corresponding common gate electrode through a corresponding gate pad.

51. The semiconductor device according to claim 41, wherein the plurality of transistor cells forms an insulated gate bipolar transistor in which the source electrode serves as an emitter and the drain electrode serves as a collector.